Amendments to the Claims

Please amend the Claims as follows and without prejudice. This listing of Claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A method for accelerating a pseudo-random input bit flow (PRBS(T_1)), generated at a first relatively low clock frequency (f1), into an identical output bit flow (PRBS(T_0)) at a second relatively high clock frequency (f0), ~~characterized in that it comprises~~ comprising:

collecting the output bit flow;

delaying the collected flow by a predetermined value (τ); and

combining the delayed flow with the input bit flow.

2. (Original) The method of claim 1, wherein delay τ is selected to respect the following relation:

$$\tau = 2^{\ell}T_1 - T_0,$$

where T_1 represents the clock period of the input bit flow, T_0 represents the clock period of the output bit flow, and ℓ is an integer setting a decimation parameter.

3. (Currently Amended) The method of claim 1 ~~or 2~~, wherein delay τ is selected to respect the following relation:

$$\tau = (2k+1)*(2^{n}-1)*T_0,$$

where k represents any integer, and where n represents the degree of the irreducible polynomial of the random sequence.

4. (Currently Amended) The method of claims ~~2 and~~ 3, wherein numbers k and ℓ respect the following relation:

$$(2k+1)*(2^n-1)+1 = p2^{\ell},$$

where p is the desired acceleration factor.

5. (Currently Amended) A circuit for accelerating an initial pseudo-random bit flow (PRBS(T_1)) generated at a first relatively low frequency (f1), into an identical accelerated bit flow (PRBS(T_0)) at a second relatively high frequency (f0), comprising a combiner [[(40)]] having a first input receiving the initial bit flow and having an output providing the accelerated flow, a second input of the combiner being connected by a delay element [[(41)]] to the combiner output.

6. (Currently Amended) The circuit of claim 5, wherein a reshaping element [[(42)]] at the high frequency is provided at the combiner output.

7. (Currently Amended) The circuit of claim 5 ~~or 6~~, wherein a phase-shifting element is further provided between the generator of the original pseudo-random bit sequence and the combiner [[(42)]].

8. (Currently Amended) The circuit of ~~any of~~ claims 5 ~~to 7~~, wherein the initial bit flow is obtained by a flip-flop generator.

9. (Currently Amended) The circuit of ~~any of~~ claims 5 ~~to 7~~, formed by optical and/or electronic means.

10. (Currently Amended) The circuit of ~~any of~~ claims 5 ~~to 9~~, wherein the delay applied by said delay element [[(41)]] is selected by implementation of the method of ~~any of~~ claims 2 ~~to 4~~.